REMARKS

Applicants respectfully request favorable reconsideration of this application, as amended.

Regarding Japanese Pub. No. 2002-197876 identified in the Office Action, Applicants note that this reference was cited and discussed in the specification at pages 1-2 and should have been considered to the extent that its relevance was discussed therein. It is presumed that the Examiner has (or will) consider the reference to the aforementioned extent. Nonetheless, to facilitate the Examiner's consideration, an English abstract of the reference is submitted herewith. Applicants respectfully request an endorsed copy of the PTO Form-1449 with the next official action, confirming that the reference has been considered.

Claims 1-10 are pending, of which Claims 1-9 have been amended herein. Claims 1-10 presently stand rejected on the merits. In particular, Claims 1-2 were rejected under 35 U.S.C. § 102(e) over Gorobets, and Claims 3-10 were rejected under 35 U.S.C. § 103(a) over Gorobets in combination variously with Tomita, Arakawa, Takata, Jeddeloh, Conley, and Sinclair.

Without acceding to the outstanding rejections, Claim 1 has been amended to set forth certain distinctive features of Applicants' invention more precisely. More generally, the claims have been editorially revised to improve clarity.

In particular, Claim 1 now recites, *inter alia*, that the first sub memory block of the first memory block includes a management area which . . . includes an area for storing linking information between said first sub memory block of said first memory block and a corresponding sub memory block of at least one other memory block. Claim 1 further recites that the control circuit performs control to read the linking information from the first sub memory block of the first memory block in accordance with the address information, and thereafter to program to the first sub memory block of the first memory block in accordance with the address information and to the corresponding sub memory block based on the linking information stored in the first sub memory block.

This combination of features is apparently not disclosed or suggested in the applied references.

For example, it is noted that Gorobets teaches a system in which each block contains data associated with a single write pointer SWP 48, as acknowledged in the Office Action. *See Gorobets*, col. 8, lines 7-10. In contradistinction, in Applicants' claimed invention the first sub memory block includes the management area that includes the linking information. See, for example, page 20, line 19 to page 22, line 25 in Applicants' specification, and Figs. 6(A) and 6(B).

Furthermore, Gorobets does not disclose or suggest a control circuit that performs control to read linking information from the first sub memory block of a first memory

block in accordance with the address information, and thereafter to program to the first sub memory block of the first memory block in accordance with address information and to the corresponding sub memory block based on the linking information stored in the first sub memory block.

The secondary references fail to remedy the aforementioned deficiencies of Gorobets with respect to the foregoing combination of features.

Therefore, Applicants respectfully request the rejections be withdrawn.

In view of the amendments and remarks presented herein, Applicants respectfully request an early Notice of Allowance.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

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WRITING METHOD FOR NON-VOLATILE MEMORY

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Abstract of **JP2002197876**

PROBLEM TO BE SOLVED: To solve such a problem that in a conventional writing method of a flash memory, as the more storage capacity of a memory array is increased, the longer length of a bit line is made, load capacity of a bit line is made larger and a time required for reaching the prescribed potential of the bit line is made longer, a time required for writing is made longer and power consumption is increased. SOLUTION: In a non-volatile memory having an AND type memory array in which plural memory cells are connected in parallel between a local bit line and a local drain line, a local drain line is precharged by supplying comparatively high voltage from a common drain line side (opposite side of main bit line), while 0 V or comparatively low voltage is applied to the main bit line in accordance with write data, after performing selection pre-charge, write voltage is applied to a word line and writing is performed, a drain current is made to flow in only a selection memory cell being desired to perform writing, and generated hot electrons are injected into a floating gate.